WEST Search History

DATE: Tuesday, July 15, 2003

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L4	((truncat$3 or delet$3 or round$3) and (buffer near3 full$3)) and (tim$3 near3 symbol$) and (equaliz$3)	18	L4
L3	((truncat$3 or delet$3 or round$3) and (buffer near3 full$3)) and (time near3 equaliz$3)	15	L3
L2	((truncat$3 or delet$3 or round$3) same (buffer near3 full$3)) and (time near3 equaliz$3)	0	L2
L1	((truncat$3 or delet$3 or round$3) same (buffer near3 full$3)) and (time near3 equaliz$3) and (symbol near3 align$4)	0	L1

END OF SEARCH HISTORY

L3: Entry 2 of 15 File: USPT May 27, 2003

DOCUMENT-IDENTIFIER: US 6570912 B1
TITLE: Hybrid software/hardware discrete multi-tone transceiver

Detailed Description Text (7):
As a receiver decoding a communication signal including multiple sub-channels carrying data, transceiver hardware 170 receives the communication signal via telephone lines 175. A conventional analog front end circuit 176 passes the received signal from telephone line 175 to an analog-to-digital converter (ADC) 178 which converts the received analog signal 178 into a series of digital samples. An optional decimator 179 decimates the series of digital samples if it is necessary to control the sample rate to a time domain equalizer. Time domain equalizer 188 performs an FIR or IIR filter operation on the digital samples from ADC 178 to partly compensate for channel impairment. In accordance with the G.992.1 (G.dmt) and G.992.2 (G.lite) or T1.413 (ANSI g.dmt), a DMT symbol corresponds to a portion of the analog signal that has a fixed duration (or number of samples) and includes a prefix that is repeated at the end portion of the DMT symbol. For G.992.2 and similar protocols, the prefix is typically removed after equalization to leave a series of a fixed length that corresponds to a DMT symbol, for example, 256 samples for the DMT symbol of the G.992.2 protocol.

Detailed Description Text (21):
Accelerator 340 writes in Rx buffer 344 the frequency domain results from the Fourier transform of received time domain samples corresponding to DMT symbols. Since G.992.2 and other DMT modulation standards are asymmetric between send and receive sub-channels, buffers 342 and 344 have different sizes and may have programmable sizes to accommodate multiple DMT protocols such as G.992.1 in addition to G.992.2. Buffers 332 and 334 serve to match the clock rate of the host (or PCI) bus to the clock rate of ASIC 300, overcome the temporary latencies (up to 1 ms) associated with the PCI bus, and accommodate the bursts of data resulting from the FFTs and IDFTs that accelerator 340 performs. Rx and Tx buffers 332 and 334 are FIFOs or dual port circular buffers with counters that track of the numbers of data words in the buffers. Each port of each buffer 332 and 334 is a read-only or write-only port, and two independent clock signals drive opposite ports. The ports on the PCI side are 32 bits (or two words) wide, and all transactions from PCI bus interface 310 are 32-bit data. The ports of buffers 332 and 334 that are coupled to accelerator 340 are 16 bits (or one word) wide, but the transactions between buffer 330 and accelerator 340 (other than "peeking" into the buffers) are usually in full DMT symbols.

Detailed Description Text (30):
The last stage of transmitter 350 applies the transmission gain and selects the proper window. More particularly, transmitter 350 includes a multiplier 356, and a memory 358 for Tx gain coefficients. Multiplier 356 multiplies the time-domain samples from IDFT engine 354 by Tx gains stored in memory 358 before transmitter 350 sends the resulting scaled samples to AFE interface 390. When selecting a window, each result is rounded to the nearest least significant bit (LSB) that is represented in the window, and clipped to avoid an overflow. Clipping generally saturates values to +/-(1-2.sup.-n), avoiding -1.

Detailed Description Text (32):
Receiver 360 includes a time-domain equalizer (TEQ) 370, a Rx magnitude block 364, a fast Fourier transform (FFT) block 380, and tone detectors 368. Receiver 360 receives the RX time domain samples from interface 390. In the embodiment of FIG. 3, the effective sampling rate, after decimation, is such that 256 samples (or 272 if a prefix is included) correspond to a DMT symbol. TEQ 370 implements a 16-tap filter

of time domain samples. TEQ 370 is post-cursor only with the main coefficient being the first coefficient, i.e., the coefficient that multiplies the most recent sample. TEQ 370 includes filter hardware 374 and memory 372 for the filter coefficients. The major sub-blocks of filter hardware 374 are a 16.times.16-bit multiplier and an accumulator. The multiplier serially performs sixteen multiplications per sample. Each multiplication determines the product of a 16-bit TEQ coefficient from memory 372 and a 14-bit sample. The accumulator sums the products to provide a filtered time-domain sample and is therefore at least 33 bits wide. The host can execute software to change one, some, or all of the TEQ coefficients in memory 372 at any time. However, changing the TEQ coefficients can interfere with operation of TEQ 370 and distort the filter results for the duration of the loading plus sixteen samples after the last coefficient was loaded.

Detailed Description Text (38):
FFT engine 386 operates on complex values in computation buffer 384 to perform the fast Fourier transform. The core FFT can be simplified because half of the input values (i.e., the imaginary parts of the input samples) are zero. FFT engine 386 can perform, a 128 point FFT with some overhead processing instead of a 256 point FFT. Once the FFT is complete, FFT engine 386 rounds and clips the required output points into the required "window", since the result is once again 16-bit only. Rounding and clipping is only required for 128 lower complex output points because for an FFT of real numbers, the upper complex points are complex conjugate of the lower ones. FFT engine 386 can implement different FFT algorithms. For example, in a linear case the input samples to the FFT engine 386 are in order whereas in a bit reversed case, the inputs to the FFT block follow a predetermined pattern and not in order. That is accomplished while copying input buffer 382 into computation buffer 384. Also, FFT engine 386 shifts the result by one bit to maximize accuracy and avoid overflows. The FFT latency is a little bit over one quarter of the DMT symbol time. To achieve this latency, FFT engine 386 has four multipliers and accumulators working in parallel and a simple finite state matching (not shown) that controls the FFT engine 386. However, the details of the implementation of the FFT engine 386 is not critical to the invention, and any FFT hardware can be used.